CLAIMS

1. (Currently Amended) A circuit for generating a plurality of phases of an input signal comprising:

a phase generator operable as a voltage controlled oscillator and as a voltage controlled delay line, said phase generator comprising a plurality of delay blocks;

a phase detector coupled in a first feedback loop with said phase generator, said phase detector for comparing said input signal with a first output signal of said phase generator when in an delay lock mode and for generating a first control signal to said phase generator to switch from said delay lock loop mode to said phase locked loop mode; and

a phase-frequency detector coupled in a second feedback loop with said phase generator said phase frequency detector for comparing said input signal with a second output signal of said phase generator when in a phase locked loop mode.

2. (Original) The circuit of Claim 1 further comprising a delay element disposed in said second feedback loop between said phase generator and said phase-frequency detector and wherein said delay element generates an output signal.

3. (Cancelled).

4. (Currently Amended) The circuit of Claim 2 ~~[3]~~ wherein said phase generator is operable for generating a plurality of phases of a second output ~~input~~ signal when operating in said phase locked loop mode.

5. (Original) The circuit of Claim 1 wherein each of said plurality of delay blocks comprises a plurality of delay elements coupled in series.

6. (Original) The circuit of Claim 5 wherein each delay block is associated with a respective multiplexer for configuring a number of said plurality of delay elements coupled in series.

7. (Currently Amended) The circuit of Claim 6 wherein a second ~~first~~ control signal generated by said phase detector causes said multiplexers to dynamically select the number of said plurality of delay elements that are coupled in series.

8. (Currently Amended) The circuit of Claim 5 wherein a second control signal generated by said phase-frequency detector controls a ~~the~~ delay time of each of said plurality of delay elements.

9. (Original) The circuit of Claim 8 wherein said circuit suppresses skew of said plurality of phases of said input signal.

10.(Currently Amended) A method for generating multiple phases of an input signal comprising:

~~a phase generator~~ accessing said input signal by a phase generator, said phase generator comprising a plurality of dynamically controlled delay blocks;

configuring said plurality of dynamically controlled delay blocks as a voltage controlled delay line in a delay lock loop mode to perform course adjustment;

generating a signal by a phase detector to cause said phase generator to operate in a phase locked loop mode; and

operating said phase generator as a voltage controlled oscillator in said phase locked loop mode for fine adjustment.

11. (Original) The method as reciting Claim 10 wherein each of said plurality of dynamically controlled delay blocks comprises a plurality of series coupled delay elements and further comprising:

coupling each set of said plurality of dynamically controlled delay blocks with a respective multiplexer wherein an output of each of said delay element is an input to said respective multiplexer.

12. (Currently Amended) The method as reciting Claim 10 wherein said delay locked loop mode varies delay elements of said dynamically controlled delay blocks until a course match is encountered using said ~~[a]~~ phase detector.

13. (Original) The method as reciting Claim 12 wherein said phase locked loop mode varies the delay of the delay elements selected in said delay lock loop mode to perform fine adjustment using a phase-frequency detector.

14. (Original) The method as reciting Claim 13 wherein said phase locked loop mode suppresses skew of a plurality of phases of said input signal.

15. (Previously Presented) A wide frequency range delay lock loop circuit comprising:

a configurable phase generator configurable;

in a first mode wherein said phase generator is coupled with a phase detector in a delay lock loop (DLL) and wherein said phase detector generates a second control signal for changing between said first mode and said second mode; and

in said second mode wherein said phase generator is coupled with a phase-frequency detector and a phase locked loop (PLL).

16. (Original) The circuit of Claim 15 wherein said phase detector compares an input signal with a signal received via a first feedback line and generates a first control signal based thereon.

17. (Original) The circuit of Claim 16 wherein said phase generator comprises:

a plurality of configurable delay blocks, each of which comprises a plurality of delay elements coupled in series.

18. (Original) The circuit of Claim 17 wherein an output of each of said delay elements comprises an input of a respective multiplexer for selectively coupling said plurality of delay elements with said first feedback line.

19. (Canceled).

20. (Original) The circuit of Claim 15 wherein said phase-frequency detector compares an input signal with a signal received from said phase generator via a second feedback line and generates a third control signal based thereon.

21. (Original) The circuit of Claim 20 wherein said phase generator further comprises:

a plurality of comfortable delay blocks, each of which comprises a plurality of delay elements coupled in series.

22. (Currently Amended) The circuit of Claim 21 wherein said control signal controls a ~~the~~ delay time of each of said plurality of delay elements.

23. (Original) The circuit of Claim 22 wherein skew of a plurality of phases of said input signal is suppressed.